

ABSTRACT OF THE DISCLOSURE

A zero power standby mode in a memory device used in a system, such as a battery powered hand held device. By disconnecting the internal power supply bus on the memory device from the external power supply during standby mode, the junction leakage and gate induced drain leakage can be eliminated to achieve a true zero-power standby mode. A p-channel field effect transistor (FET) may be used to gate the external power supply such that the internal power supply bus on the memory device may be disconnected from the external power supply.

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